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REDUCED NUMBER OF POWER SWITCHES IN MULTI LEVEL INVERTER USING SPWM TECHNIQUE TO MITIGATE FOR SAG AND SWELL

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ABSTRACT

The study objective is to design and implement new topology symmetric for 3phase by focusing on reduced number of semiconductor devices in nine level Hybrid cascaded H-bridge multilevel inverter based on DVR. The main aim of this paper is to increase the number of levels with a low number of power switches and at the output without adding any complexity to the power circuit. The proposed work in inverter can generate odd level and it is used in SPWM technique for generating pulses. The main advantage of the new topology includes reduced switches from 48 to 36 and mitigation of sag, swell, analysis of the total harmonic distortion (THD), power factor improvement and high output voltage. The proposed topology results in reduction of occupied area, cost and simplicity of control system and it is well-suited for high application. The performance of proposed work can be analysed through Matlab/simulink software. Finally, the results are compared at output side THD and PF conventional type and new topology is devised.

KEYWORDS: Nine Level hybrid Cascaded H-Bridge Multilevel Inverter, DVR, SAG, SWELL, THD, Power Factor Improvement & SPWM.

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Original Article

INTRODUCTION

Generally, inverters in circuit or device that converts DC to AC. Disadvantage of inverter includes its less efficiency, high cost and high switching losses. To overcome these disadvantages we choose multilevel inverter(MLI). MLI is an excellent circuit for power conversion system for high voltage and good power quality applications. In this MLI huge number of power switches are used and number of levels increases so harmonics are reduced(1). The concept of multilevel inverter (MLI) has been introduced in since 1975. The cascaded H-Bridge multilevel inverter(CHMLI) was first proposed in 1975. In recent years, multi level inverters are used for high power,high voltage applications and output of multi level inverters generate staircase output waveform. This waveform is like sinusoidal waveform. The CHMLI is very easy compared to other MLI like diode clamped MLI and flying capacitor MLI(2).

There are two methods used in MLI control method (a) Fundamental switching frequency and (b) high switching frequency. For high switching frequency classified as Sinusoidal pulse width modulation(SPWM),Space Vector Pulse Width Modulation(SVPWM), Selective Harmonics Pulse Width Modulation(SHPWM). Among these PWM methods SPWM is most used for the MLI because it is very simple and easy to implemented (3).

This proposed work has been used in SPWM technique. Power switches like IGBTs are used in hybrid CHMLI because both features of BJT and MOSFET are added to the IGBT. It is a fast switching capability (4).

Nonlinear loads have generated harmonics in the power supply systems and power electronics based applications that draw non sinusoidal current and voltage creating voltage distortion or huge disturbances in loads. In recent times, various publications have appeared on harmonics like on sag and swell, reactive power load balancing and neutral current compensation related with linear and non linear loads. MLI can overcome these drawbacks easily (5).

MLI features of multilevel structure are as follows. With reduction in harmonics, the number of levels increases, thus reducing filtering requirements and avoiding switching losses because the devices are switched to low frequency as they gain higher efficiency(6).

This paper aims at reducing semiconductor devices and DC sources in CHMLI because it is a big disadvantage in conventional 9 levels CHMLI. Reduced power switches in 9 level CHMLI reduces its cost, and THD and complexity are also automatically reduced. Another purpose is to mitigate sag and swell harmonics, generate low THD and improve the power factor (7).

The power quality of electrical power delivered is characterized by two factors namely 1)continuity of supply and 2) quality of voltage. Power quality is a concept of powering and grounding sensitive equipment in a manner that is suitable to operation of the equipment(8)**.**

Power Quality Problems

There are many reasons by which the power quality is affected. Voltage Sag, Swell and THD. The occurrence of such problems in the power system network is almost in dispensable(9). Therefore, to maintain the quality of power care must be taken that suitable devices are kept in operation to prevent the consequences of these problems.

(A) Voltage Sag: A voltage sag is a short duration decreases in voltage in voltage values.

Causes: Short circuits and load additions in customer service area.

(**B) Voltage Swell:** A voltage swell is a short duration in voltage values.

Causes: Large load changes and power line switching.(10)

TOTAL HARMONIC DISTORTION

It is defined as the ratio of the equivalent root mean square (RMS) voltage/current of all harmonic frequencies over the RMS voltage / current of the fundamental frequency is the main frequency of the signal.

DYNAMIC VOLTAGE RESTORER (DVR)

DVR is a custom power device which is connected to the distribution or transmission lines in series between source supply and load. It is power electronic based static device and it consists of i) voltage source converter(VSC),ii) Coupling Transformer (T/F), iii) Filter circuit and iv)Control unit

Advantages of DVR

Simple, Low cost, Small Size, Fast, Dynamic Response and flexible Efficient Solution.(11)

Operating Principle

The principle operation of DVR is that it injects a voltage waveform through an injection transformer that is the

difference between pre-sag and sagged voltage.

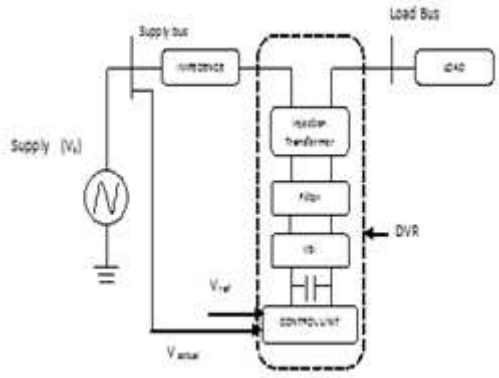

Figure 1: DVR Block Diagram

CONVENTIONAL MULTILEVEL INVERTER

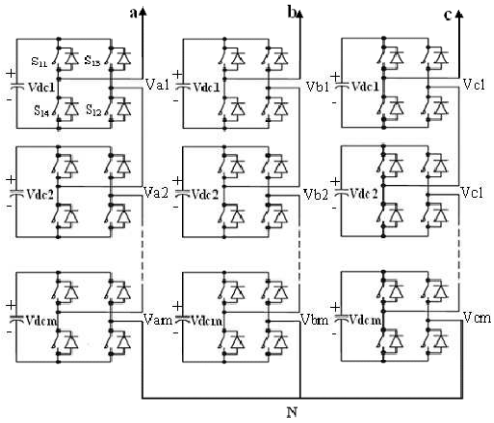

Figure 2: Conventional Type of Cascaded MLI M Level Inverter

Figure 2shows the configuration of cascaded multilevel inverter, the full bridge configuration with a separate DC source, which may be batteries, fuel cells or solar cells and are connected in series [5],[9]. Each full bridge inverter (FBI) unit can generate a three level output: +Vdc, 0 or –Vdc by connecting the DC source to the AC load side by different combinations of the four switches S1, S2, S3 and S4. Using the top level as example, turning on S1 and S4 yields +Vdc output. Turning on S2 and S3 yields -Vdc output. Turning off all switches yields 0 volts output. The AC output voltage at other levels can be obtained in the same manner. The number of voltage levels at the load generally defines the number of FBIs in cascade. If N is the number of DC sources, the number of output voltage levels is m=2N+1. The number of FBI units *N* is (m-1)/2. Where, m is the sum of the number of positive, negative and zero levels in multilevel inverter output. The number of converters *N* also depends on: 1) the injected voltage and current harmonic distortion requirements 2) the magnitude of the injected voltage required and 3) the available power switch voltage ratings [8]. The AC load rating and therefore the DC source rating depend upon the total compensation voltage required. The main features of cascaded multilevel inverters are:

- For real power conversions from DC to AC, the cascaded inverters need separate DC sources and it is separate well suited for various renewable energy sources such as fuel cell, photovoltaic and biomass.
- Least number of components are required to achieve the same number of voltage levels.

- Optimized circuit layout and packaging are possible.
- Soft-switching techniques can be used to reduce switching losses and device stresses.

SPWM TECHNIQUE

High power application low output distorted. Gating signals are generated by comparing a rectangular reference signals of amplitude Er with a triangular carrier wave of amplitude Ec. The fundamental frequency of output voltage is determined by the frequency of the reference signal. The pulse width p varying Er from 0 to Ec.

The ratio of Er to Ec is the control variables and is defined as the amplitude Modulation Index(M).

$M = E_R / E_C$, $M<1$

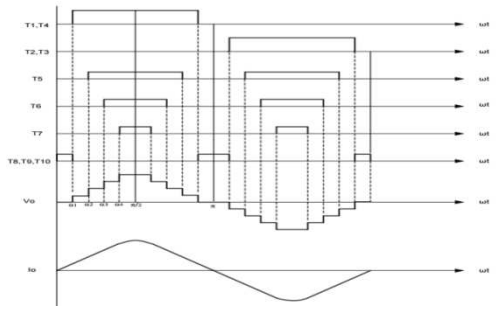

Figure 3: Switching Pulses of Nine Level Inverter

PROPOSED SYSTEM WORKING PRINCIPLE

New Topology: Symmetric Type

DVR had been constructed with hybrid nine-level cascaded H-bridge multilevel inverter was designed in this section. This system is consisting of 3 phase supply. Figure.4 and Figure. 6 are modelled in MATLAB/Simulink environment along with a sim power system toolbox. DVR is a power quality circuit used for reduced sag, swell for power quality improvement.

At 0.1s, the supply voltage is distorted and continued for 9 cycles. At 0.1s,a sag in supply voltage is created for 9 cycles, and at 0.2s, a swell in the supply voltages is created for 9 cycles. It is observed that the load voltage is regulated to constant amplitude under both sag and swell conditions. The load voltage is maintained sinusoidal by injecting proper compensation voltage by the DVR.

New topology used to realize the VSC, multilevel inverter technology. Multilevel converters can realize high power and high voltage using low semiconductor switches of relative small ratings while avoiding the voltage and current sharing problems associated with series and parallel connection.

In this proposed work 36 switches are used at nine level CHMLI.

Equation

m = No. of voltage sources (In this paper 12 dc sources are used)

No of legs = 3 nos.

No. of switches = No of legs *No. of voltage sources

= 3*12=36 nos.

No of Levels = 2N+1 = 2(4)+1 = 9

Where, N=Number of inverter's connected in either in series or parallel.

Harmonics are reduced by filters these are also designed in this diagram. Proposed work followed symmetric type, it is known as all DC voltage sources are same value is considered(i.e. 40vots).

- Conventional type of DVR 9 level CHMLI THD is 2.13% and Power Factor is 0.9998. [48 swithces used]
- Proposed work (new topology) DVR 9 level CHMLI THD is 1.96%and Power Factor is 1.[48 swithces used]

From below Table2 switch states of 9 level proposed topology for one legfrom this data with proposed work (new topology) nine level cascaded H inverter is more eficient or excelent procedure for compensate the power quality problems compared to the conventional type of DVR 9 level CHMLI.

SIMULATION RESULTS

I. Simulation with Conventional Type with DVR

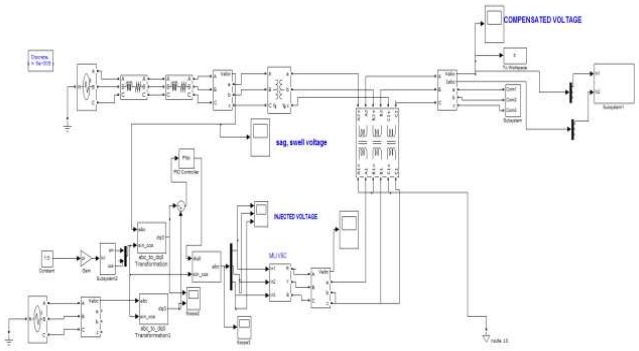

Figure 4: DVR With Hybrid 9 level cascaded Multi Level Inverter (48 Switches Used In Hybrid CHMLI-Conventional Type)

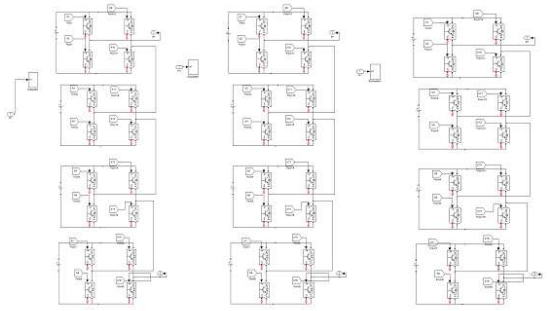

Figure 5: Conventional Type Simulation Design of Cascaded H-Bridge Nine-Level Inverter with SPWM (48Switches)

II. Simulation with New Topology Type with DVR

Proposed Work (New Topology Type)

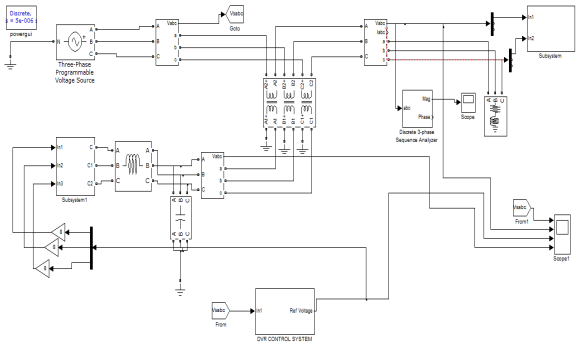

Figure 6: Main Diagram of DVR with Reduced Semiconductor Devices in Hybrid 9 Level Cascaded Multi Level Inverter (36 Switches are Used In Hybrid CHMLI-Proposed Work)

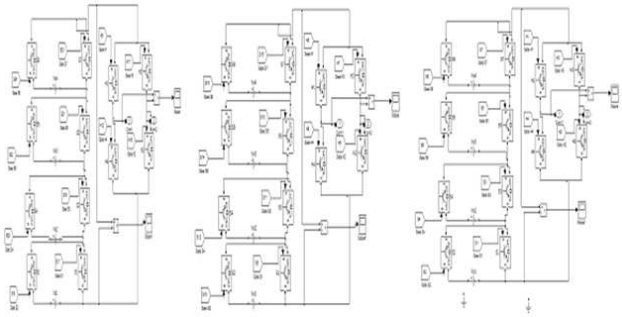

Figure 7: Proposed Work of New Topology Type Simulation Design of Hybrid 9 Level Cascaded H-Bridge Multi Level Inverter with SPWM (36 Switches)

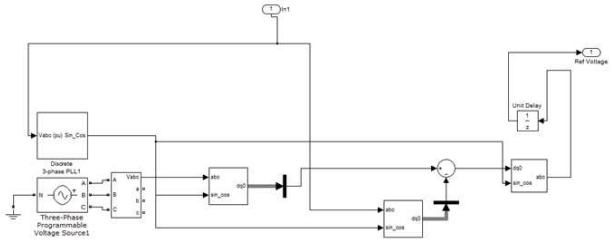

Figure 8: Proposed Work Simulation of SPWM for Estimated the Reference Voltage(i.e.New Toplogy)

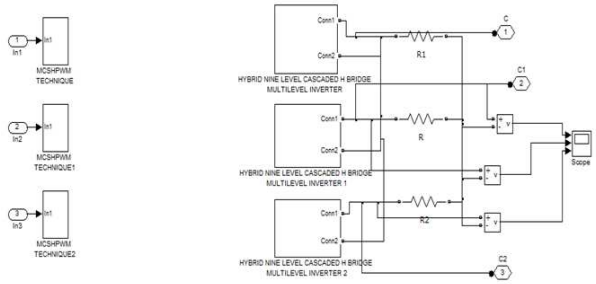

Figure 9: Proposed Work Simulation of Subsystem (Three Blocks give Three Legs)

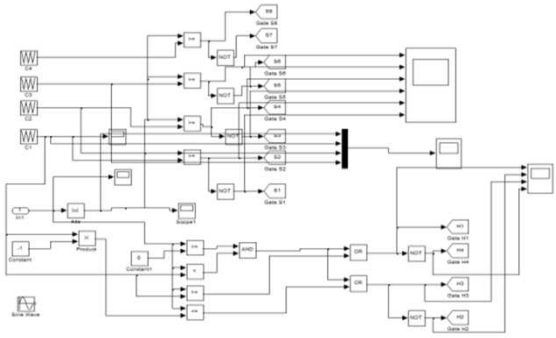

Figure 10: Proposed Work Simulation with Comparion and Generated Pulses (Spwm Technique) (In Proposed Work Three Same Circuits are Developed)

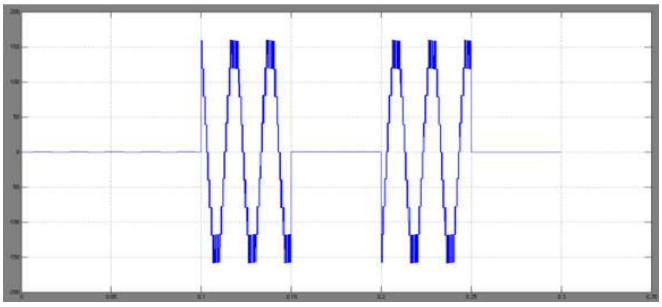

Figure 11: Proposed Work Output Voltage of VSC (Voltage of Hybrid Cascaded H-Bridge Nine-Level Inverter)

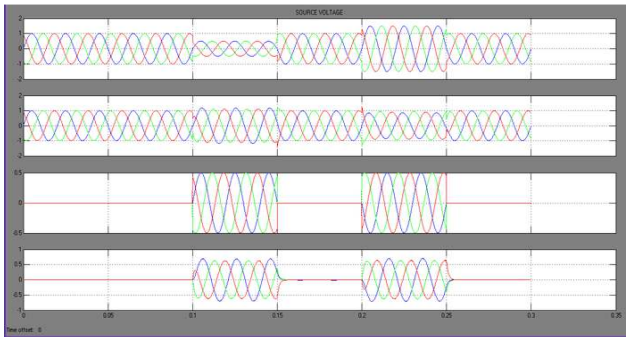

Figure 12: Proposed Work Results Shows the Voltage Sag and Swell, Load Voltage, Injecting Voltage and Reference Voltage

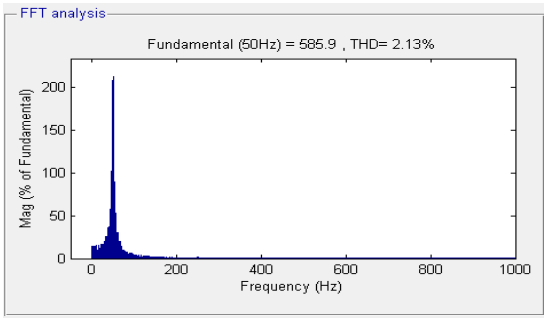

Figure 13: Convention Type FFT Analyses (48 Switches in 9 Level CHMLI)

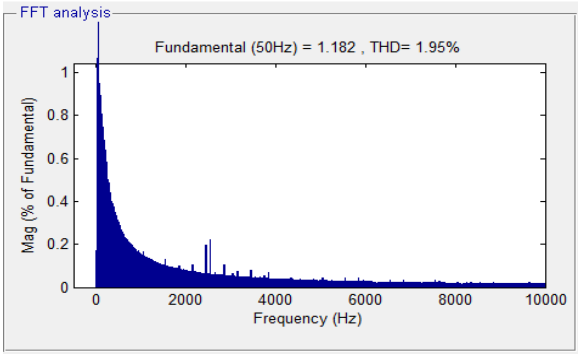

Figure 14: Proposed Work FFT Analyses (36 Switches in Hybrid 9 Level CHMLI)

Table 1: Switch States of 9 Level Proposed Topology (One Leg)

S1	S2	S3	S4	S5	S6	S7	S8	H1	H2	H3	H4	Voltage level at Vo load	Voltage level at Vo load
1	0	1	0	1	0	0	1	1	1	0	0	(Vdc1)	+Vdc
0	1	1	0	1	0	0	1	1	1	0	0	(Vdc1++Vdc4)	+2Vdc
0	1	0	1	1	1	1	0	1	1	0	0	(Vdc2+Vdc3+ Vdc4)	+3Vdc
0	1	0	1	0	1	0	1	1	1	0	0	(Vdc1+Vdc2+ Vdc3+Vdc4)	+4Vdc
0	0	0	0	0	0	0	0	1	0	1	0	(0)	0
1	0	1	0	1	0	1	0	0	0	1	1	-(Vdc4)	+Vdc
0	1	1	0	1	0	0	1	0	0	1	1	-(Vdc4+Vdc1)	+2Vdc
0	1	0	1	0	1	1	0	0	0	1	1	-(Vdc2+Vdc3 +Vdc4)	+3Vdc
0	1	0	1	0	1	0	1	0	0	1	1	-(Vdc1+Vdc2 +Vdc3+Vdc4)	+4Vdc

Table 2: SPWM Technique

S.NO	TYPE	No of switches	THD%	PF
1	Conventional Type	48	2.13	0.9994
2	New Topology (Proposed work)	36	1.96	1

CONCLUSIONS

In this paper, symmetric hybrid 9 level cascaded H-Bridge multilevel inverter is proposed in DVR. Power switches are reduced in new topology of multilevel inverter. The proposed structure can be discussed in Table1 and Figure 7. This type of MLI is more preferred in industries because installation area less, reduced cost and simple circuit. The voltage output is verified confirm this type of symmetric new topology is good performance. Proposed work MLI used to mitigate sag, swell, and improve the power factor and THD by using SPWM technique. This proposed work suited for a high voltage application. THD is very low, and a good power factor and compared to the convention type of MLI. This new topology performance can be analyzed through Matlab/simulink software. Design of proposed system for power quality improvement in distribution lines.

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11. *A New Basic Unit for Symmetric and Asymmetric Cascaded Multilevel Inverter with Reduced Number of Components Ebrahim Babaei1, Member, IEEE, Maryam Sarbanzadeh2, Student Member, IEEE, Mohammad Ali Hosseinzadeh3, Carlo Cecati4, Fellow, IEEE 1, 2, 3 Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran 4Department of Information Engineering, Computer Science and Mathematics, University of L'Aquila, L'Aquila, Italy E-mails: e-babaei@tabrizu.ac.ir; maryam_sarbanzadeh@yahoo.com; m.a_hosseinzadeh@yahoo.com; carlo.cecati@univaq.it*
12. *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) ISSN: 2278-1676 Volume 2, Issue 6 (Sep-Oct. 2012), PP 26-36 www.iosrjournals.org www.iosrjournals.org 26 | Page **New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources** M. Kavitha1, A. Arunkumar 2, N. Gokulnath 3, S. Arun 4 1Assistant Professor/ Dept. of Electrical Engineering, 2, 3, 4 Final year students / Dept. of EEE / DR.S.J.S Paul Memorial College of Engineering & Technology / Pondicherry / India*
13. *cascaded and hybrid MLI with reduced number of switches for IM by M.MURUGUSAN Journal name :JEE*
14. *A New basic unit for Symmetric and Asymmetric Cascaded Multilevel Inverter with Reduced Number of Components 978-1-5090-3474-1/16/$31.00@2016 IEEE*

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